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100	100

[illegible]

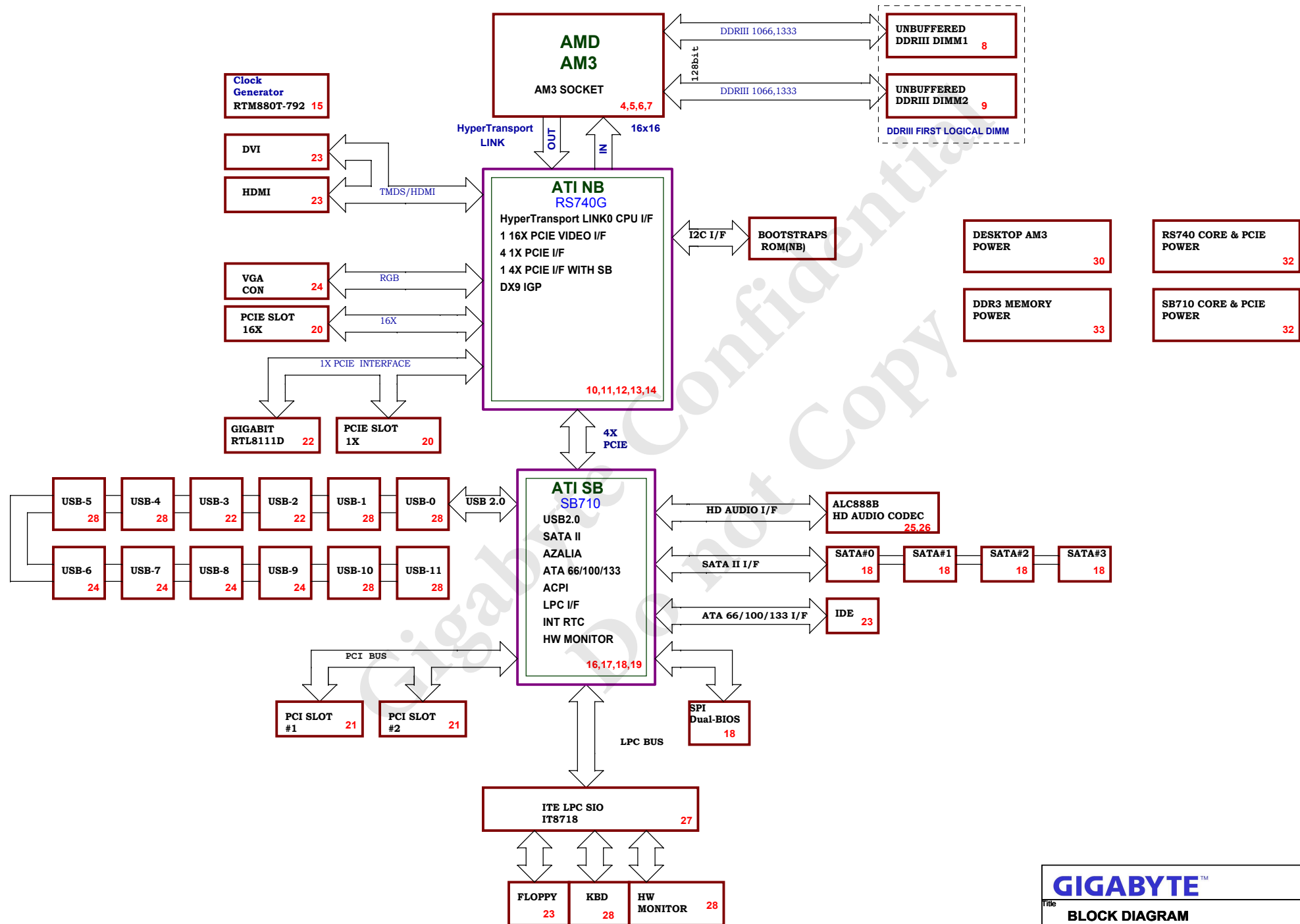
P-Code: U98102-0

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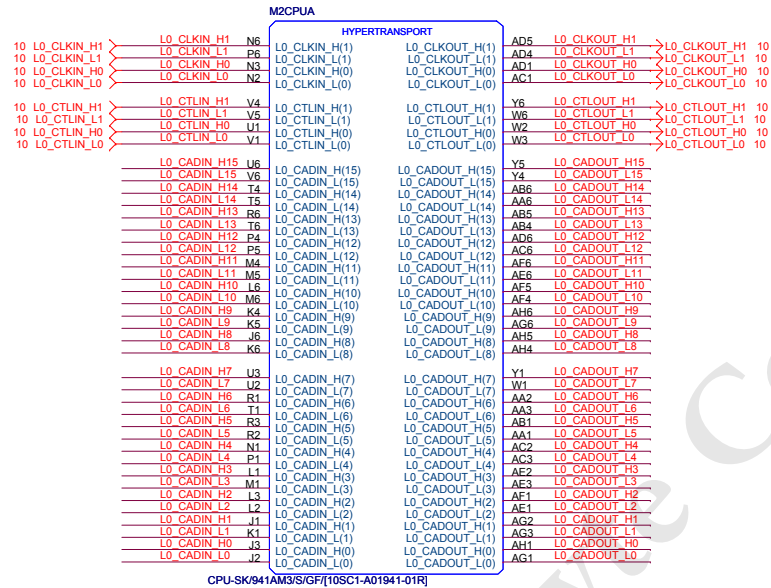
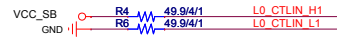
Circuit or PCB layout change for next version

[illegible]

RS740 CUSTOMER DESKTOP REFERENCE DESIGN



L0_CADIN_L[0..15] < L0_CADIN_L[0..15] 10
 L0_CADIN_H[0..15] < L0_CADIN_H[0..15] 10
 L0_CADOUT_L[0..15] < L0_CADOUT_L[0..15] 10
 L0_CADOUT_H[0..15] < L0_CADOUT_H[0..15] 10

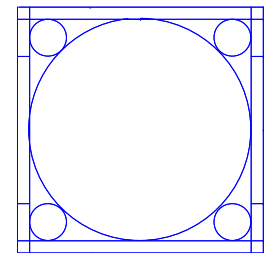


CPU_VDD_RUN = VCORE
 CPU_VDDA_RUN = VDDA25
 VLDT_RUN = VCC12_HT
 CPU_VDDIO_SUS = DDR15V
 CPU_VDDR = CPU_VDDR12

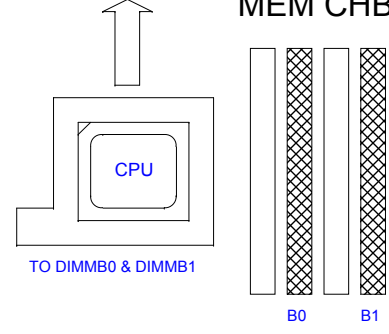
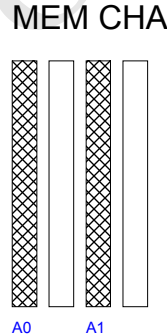
VLDT_A = VCC12_HT
 VLDT_B = HT12B

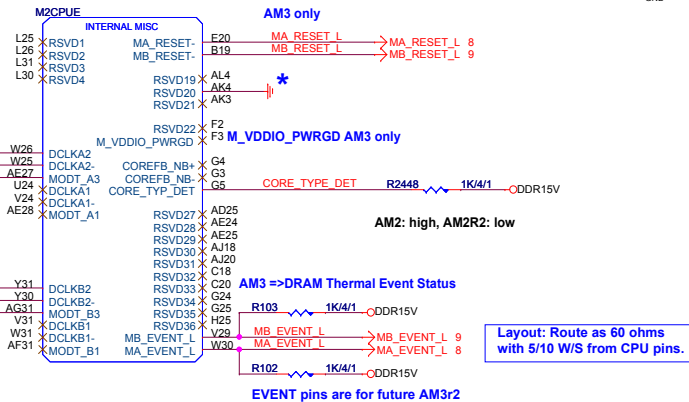
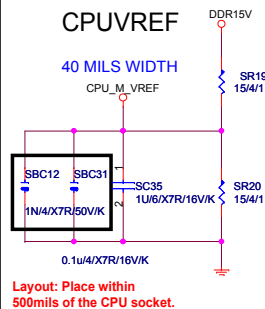
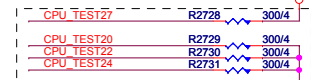
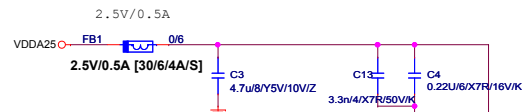
M2CPU

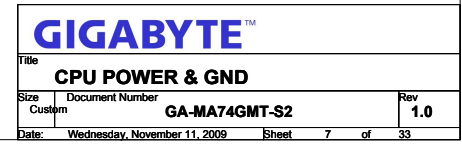
AM2RM/PP/BU/PB[12KRC-04K812-11R]


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Title			
CPU HYPER TRANSPORT			
Size	Document Number	Rev	
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MODT_A[0..3] ↔ MODT_A[0..3] 5,6
-DQSA[0..8] ↔ -DQSA[0..8] 5
DQSA[0..8] ↔ DQSA[0..8] 5
DMA[0..8] ↔ DMA[0..8] 5
MA_CK[0..7] ↔ MA_CK[0..7] 5

SMBDATA
SMBCLK
C205 100p4/NPO/50V/J/X
C206 100p4/NPO/50V/J/X

DDR15V
Trace min 10/10
R101 154/1 VREFDQ_A
R23 154/1
R24 154/1
Trace min 10/10
R2 VREFCA_A

C278 0.1u4/5V/16V/Z
C279 0.1u4/5V/16V/Z
C280 0.1u4/5V/16V/Z

9,15,17,30,31 SMBCLK
9,15,17,30,31 SMBDATA
VCC3 0

5 SBA2 SBA2 52 BA2
5 SBA1 SBA1 190 BA1
5 SBA0 SBA0 71 BA0

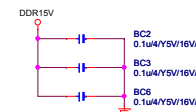
5 CKEA1 CKEA1 169 CK1
5 CKEA0 CKEA0 50 CK0
5 CSA3 CSA3 76 S1+
5 CSA2 CSA2 193 S0

5 DCLKA3 DCLKA3 64 CK1/NU
5 DCLKA3 DCLKA3 63 CK1/NU
6 DCLKA2 DCLKA2 185 CK0
6 DCLKA2 DCLKA2 184 CK0

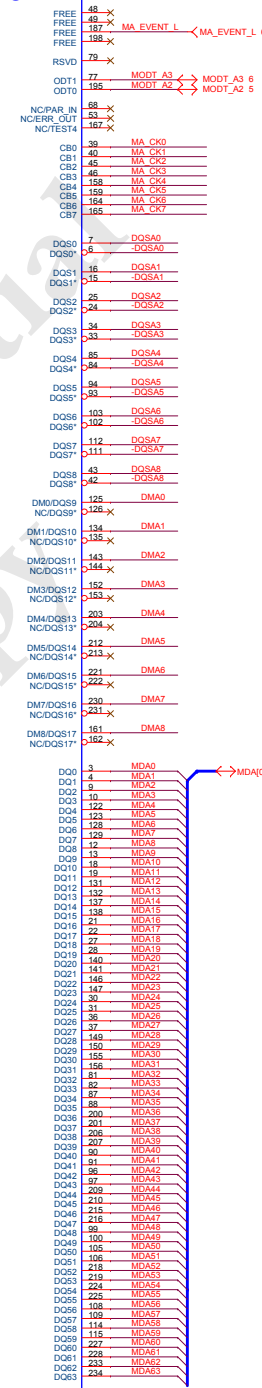
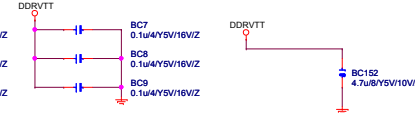
5 MAA[0..15] ↔ MAA[0..15]
MAA0 188 A0
MAA1 181 A1
MAA2 61 A2
MAA3 180 A3
MAA4 59 A4
MAA5 58 A5
MAA6 178 A6
MAA7 56 A7
MAA8 177 A8
MAA9 175 A9
MAA10 70 A10/AP
MAA11 65 A11
MAA12 174 A12
MAA13 186 A13
MAA14 172 A14
MAA15 171 A15

6 MA_RESET L MA_RESET L 168 RESET+
5 -SCAS0 -SCAS0 174 CAS+
5 -SRAS0 -SRAS0 192 RAS+
5 -SWEA -SWEA 73 WE+

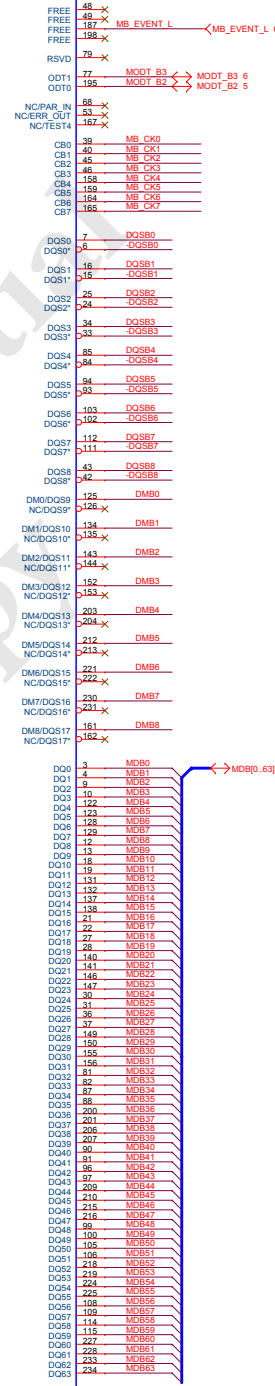
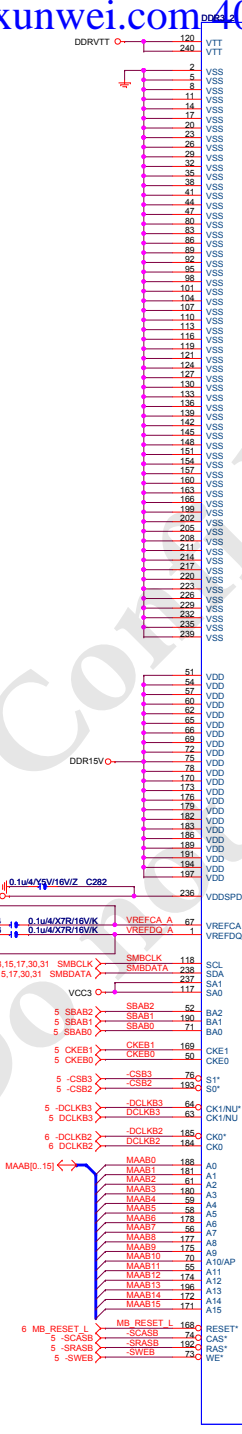
DDR15V Decouple



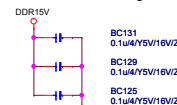
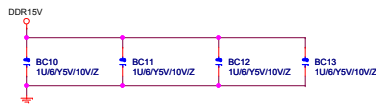
DDRVTT Decouple

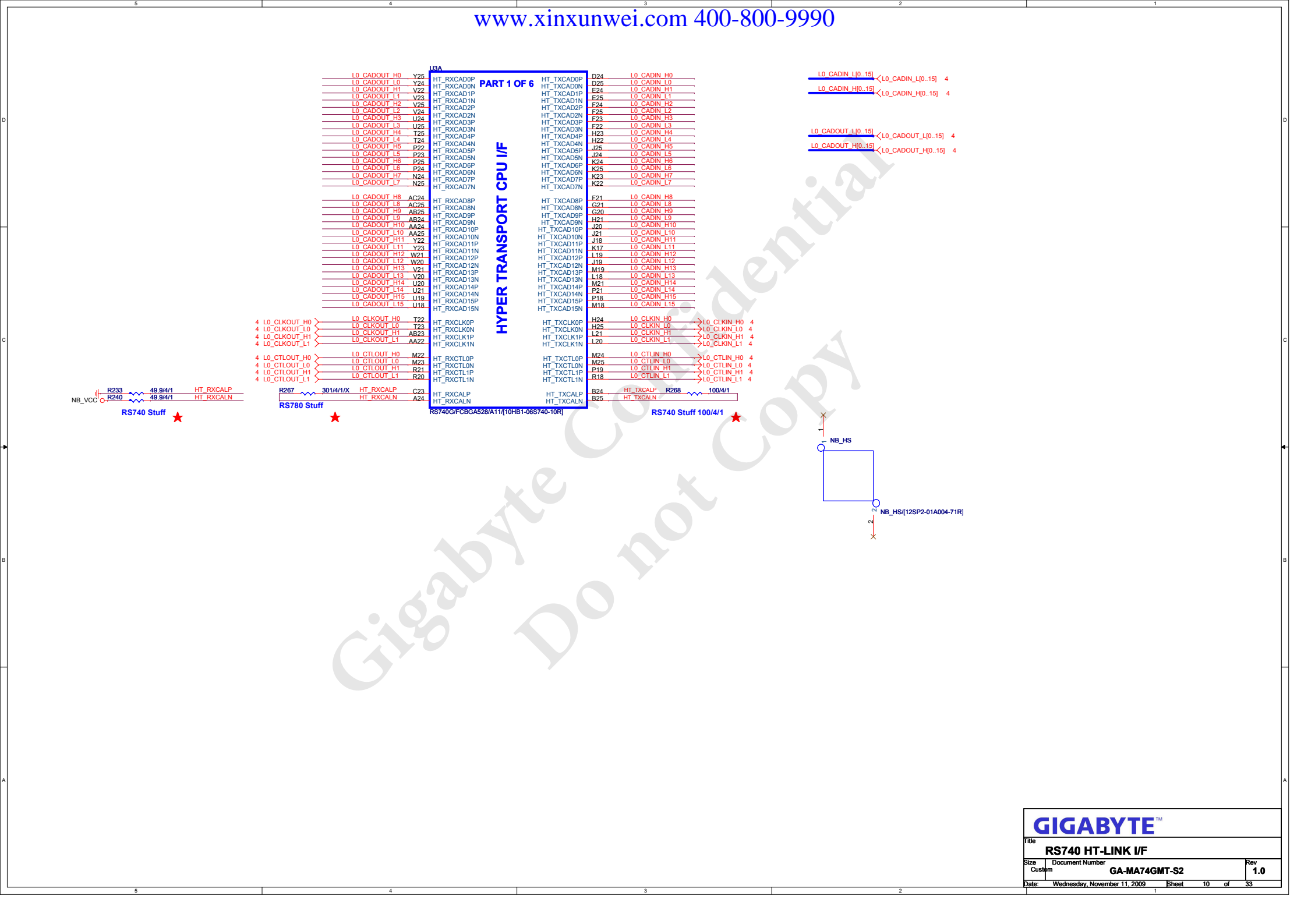


-DQS[0..8] <-> DQS[0..8] 5
DQS[0..8] <-> DQS[0..8] 5
DM[0..8] <-> DM[0..8] 5
MODT_B[0..3] <-> MODT_B[0..3] 5.6
MB_CK[0..7] <-> MB_CK[0..7] 5



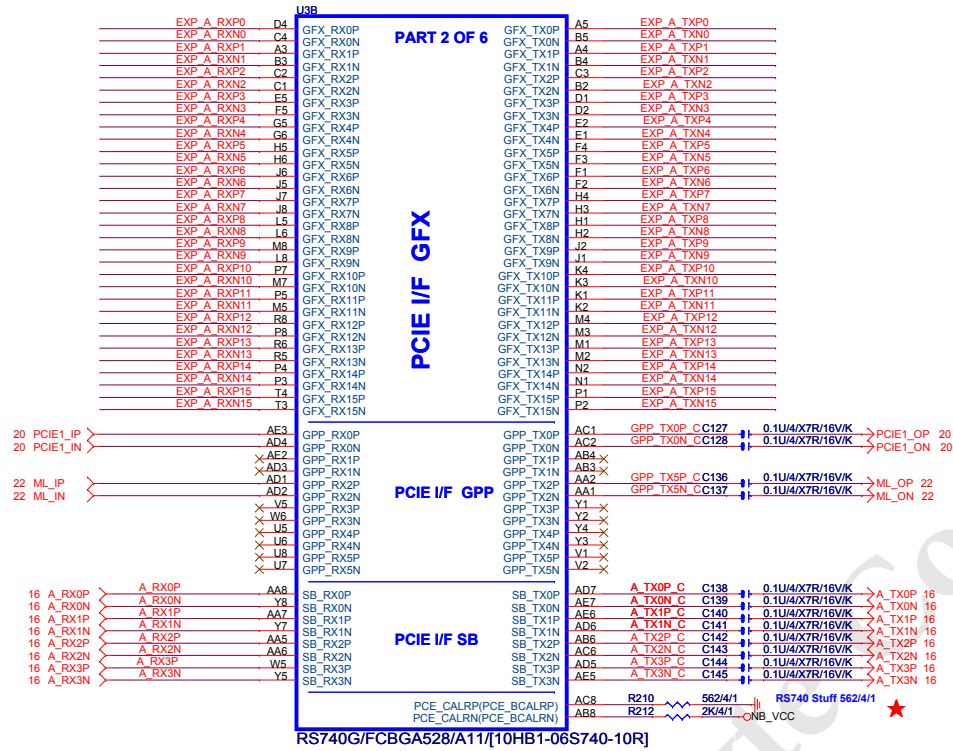
DDR15V Decouple

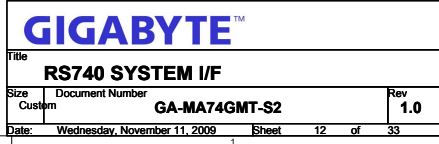


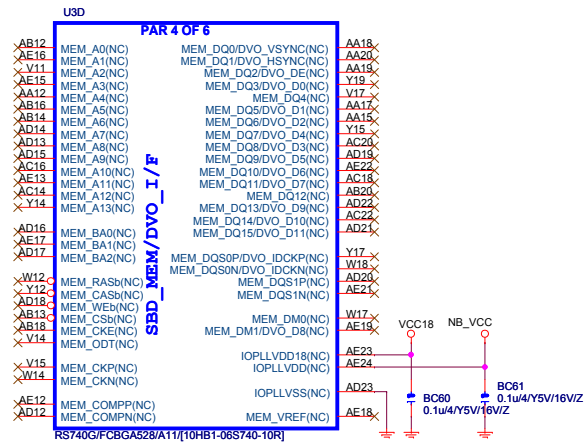


EXP_A_RXP[0..15] >>> EXP_A_RXP[0..15] 20
EXP_A_RXN[0..15] >>> EXP_A_RXN[0..15] 20

EXP_A_TXP[0..15] >>> EXP_A_TXP[0..15] 20
EXP_A_TXN[0..15] >>> EXP_A_TXN[0..15] 20







RS740/RX780/RS780 STRAPS

Note: for RS780, change R232 to 150R as AUX_CAL, place close to pin C8

12 RS740_DFT_GPIO1 >> R272 RS740 non-Stuff

Note: for RX780, R217 (RX780_DFT_GPIO1) to 3K accordingly

12,24 DAC_VSYNC << R276 RS780 Stuff 3K/4/1X

12 RS740_DFT_GPIO5 >> R280 RS740 Stuff 3K/4/1

Note: for RX780, change following pull-down resistor to 3K accordingly
R912 (RX780_DFT_GPIO5)

Note: for RX780, change following pull-down resistor to 3K accordingly
R913 (RX780_DFT_GPIO4)
R218 (RX780_DFT_GPIO3)
R911 (RX780_DFT_GPIO2)

12 RS740_DFT_GPIO0 >> R288 RS740 Stuff 3K/4/1

12,24 DAC_HSYNC << R285 RS780 Stuff 3K/4/1X

Note: for RX780, change following pull-down resistor to 3K accordingly
R219 (RX780_DFT_GPIO0)

RS740/RX780/RS780: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS740: pin DFT_GPIO1

RX780: pin DFT_GPIO1

RS780: pin SUS_STAT#

RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO and/or memory IO

1 : Disable (RS740/RS780); Enable (RX780)

0 : Enable (RS740/RS780); Disable (RX780)

RS740: pin DFT_GPIO5

RX780: pin DFT_GPIO5

RS780: pin VSYNC

RS740: STRAP_PCIE_SB/GPP_CFG[2:0] (Pins: RS740_DFT_GPIO[4:2])

These pin straps are used to configure PCI-E GPP mode.

111: register defined (register default to Config E) default

110: 4-0-0-0-0 Config A

101: 4-4-0-0-0 Config B

100: 4-2-2-0-0 Config C

011: 4-2-1-1-0 Config D

010: 4-1-1-1-1 Config E

others: register defined (default to Config E)

RX780: STRAP_PCIE_GPP_CFG[2:0] (Pins: RX780_DFT_GPIO[4:2])

111: 1-1-1-1-1 Mode L default

110: 1-1-1-1-1 Mode L

101: 2-0-2-0-2-0 Mode C2

100: 2-0-2-0-1-1 Mode K

011: 2-0-1-1-1-1 Mode E

010: 1-1-1-1-1-1 Mode L

001: 4-0-0-0-1-1 Mode C

000: 4-0-0-0-2-0 Mode B

RS780: STRAP_PCIE_GPP_CFG[2:0] (configure thru register setting)

1-1-1-1-1-1 Mode L default

1-1-1-1-1-1 Mode L

2-0-2-0-2-0 Mode C2

2-0-2-0-1-1 Mode K

2-0-1-1-1-1 Mode E

1-1-1-1-1-1 Mode L

4-0-0-0-1-1 Mode C

4-0-0-0-2-0 Mode B

RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

Enables Side port memory

1. Disable (RS740/RS780)

0 : Enable (RS740/RS780)

RS740: pin DFT_GPIO0

RS780: pin HSYNC

RX780: Not Applicable

RX780/RS780: STRAP_DEBUG_BUS_PCIE_ENABLE

Enables Test debug bus

using PCIE bus

1. Disable (can be enabled

thru nbcfg register)

0 : Enable

RX780: pin DFT_GPIO0

RS780: configurable thru register

setting only

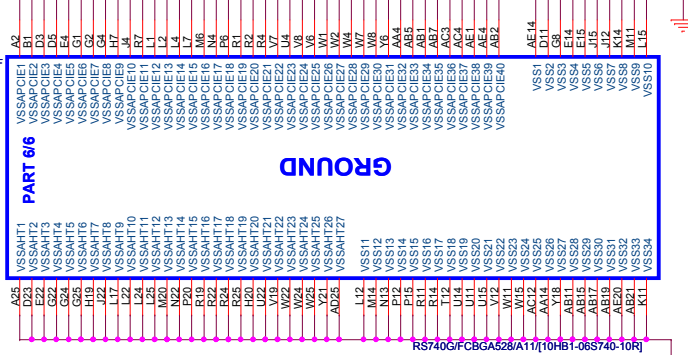
RS740: Not supported

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Title		
RS740 STRAP		
Size	Document Number	Rev
Custom	GA-MA74GMT-S2	1.0
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RS740/RX780/RX780 POWER DIFFERENCE TABLE						
PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC
VDD33	+3.3V	NC	+3.3V	VDDLTP18	+1.8V	NC
IOPLLVD18	+1.8V	NC	+1.8V	VDDLTP18	+1.8V	NC

GROUND

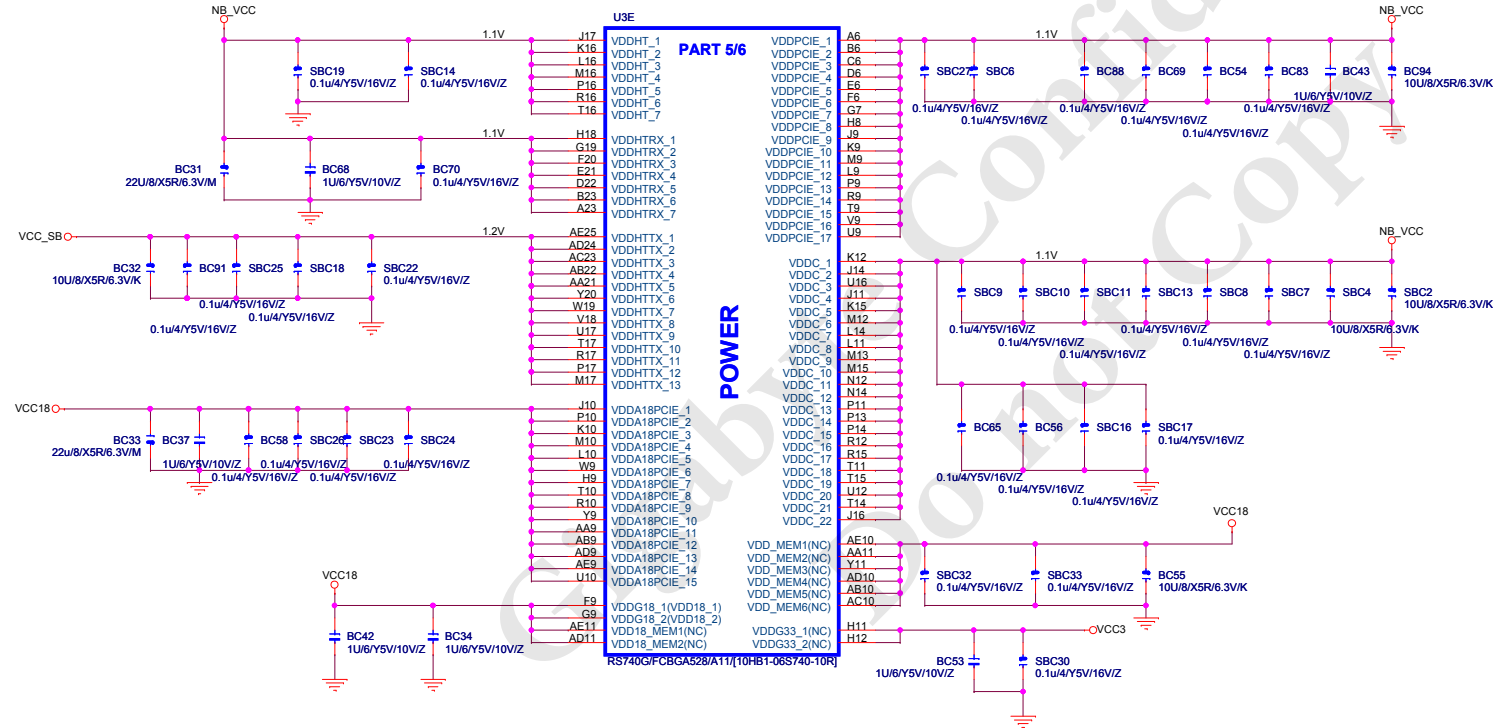


Please use 1mm pad size,
place all ELT test pads
on bottom side only

PART 5/6

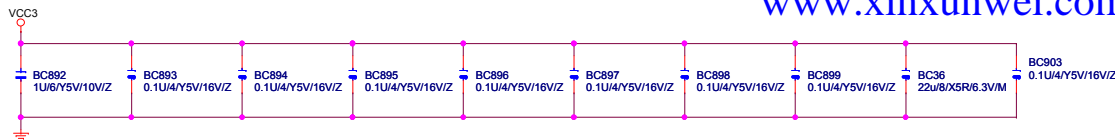
POWER

RS740G/FCBGA528/A11(10HB1-06S740-10R)



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Title RS740 POWER & GND		
Size Custom	Document Number GA-MA74GMT-S2	Rev 1.0
Date: Wednesday, November 11, 2009 Sheet 14 of 33		

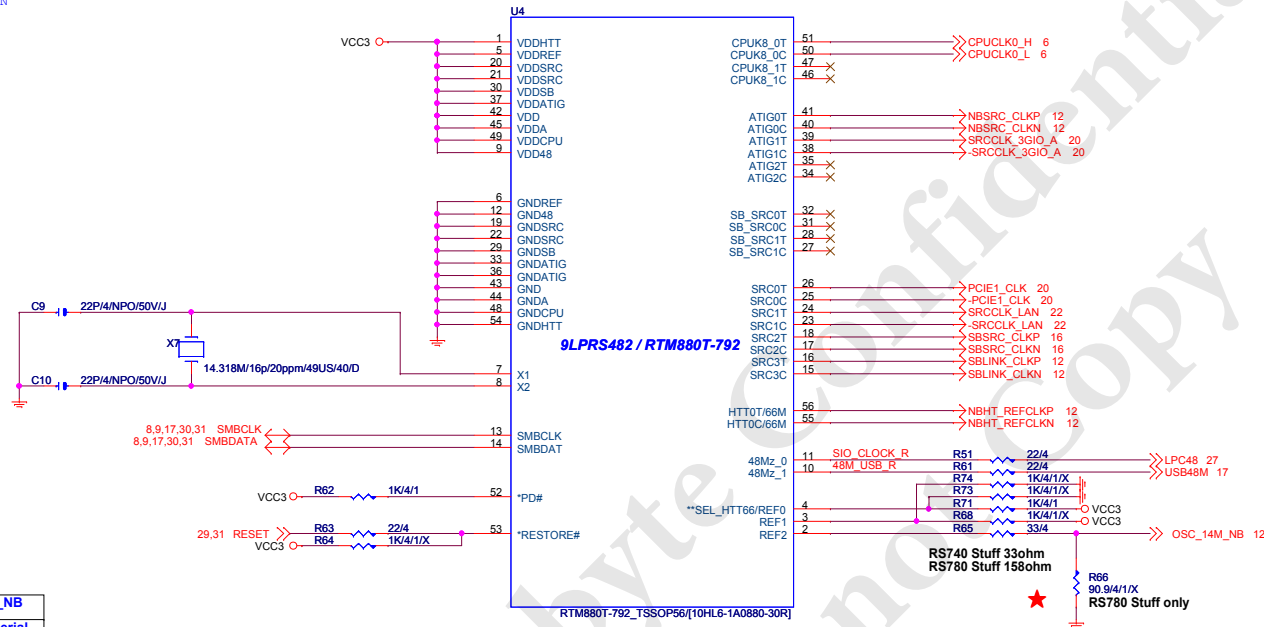


- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

NB/CPU INPUT TABLE

NB CLKs	RS740	RX780	RS780
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* the GFX_REFCLK input is required for all cases



Watch dog --
RESTORE# 接 RESET

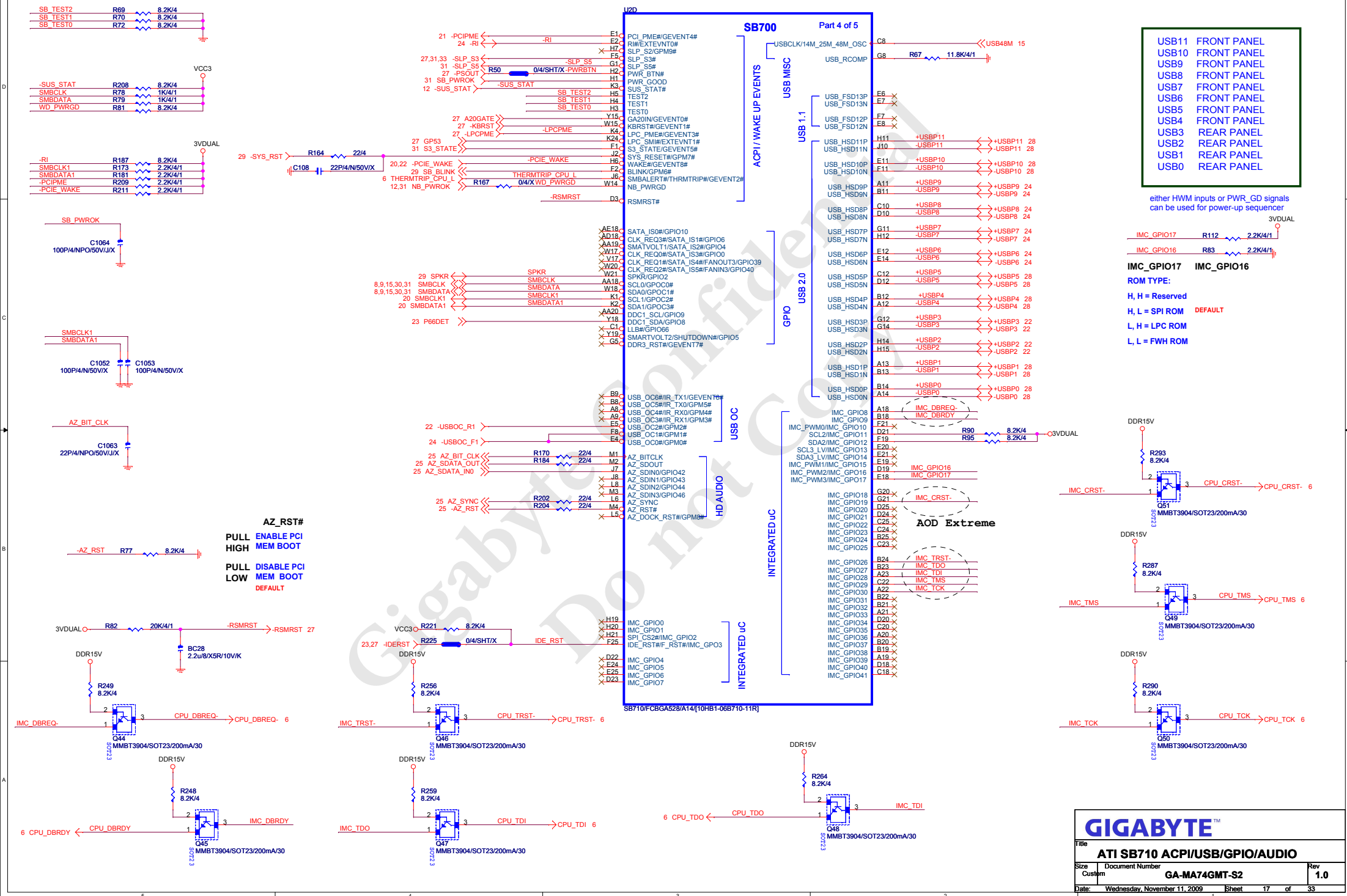
	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

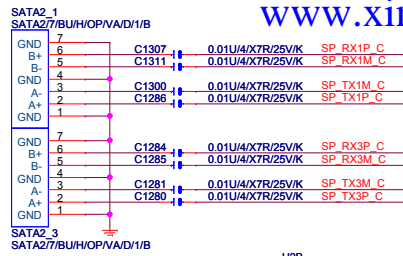
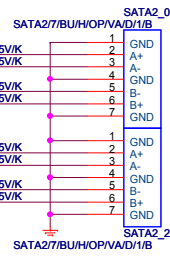
REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

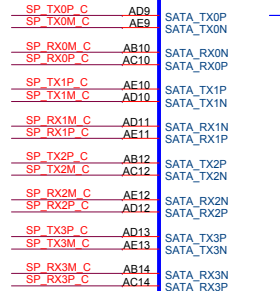
GIGABYTE™

Title	RTM880T-792		
Size	Document Number	Rev	
Custom	GA-MA74GMT-S2	1.0	
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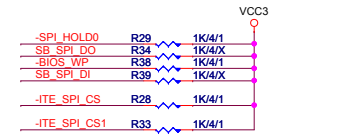
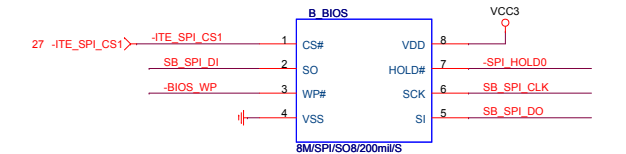
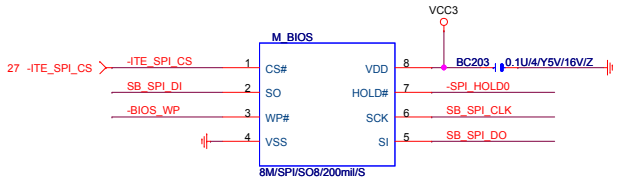
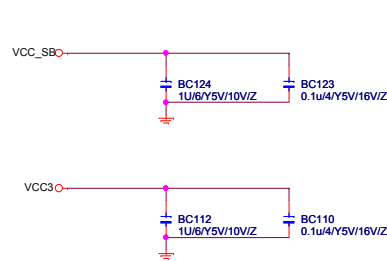




PLACE SATA AC COUPLING
CAPS CLOSE TO SB600

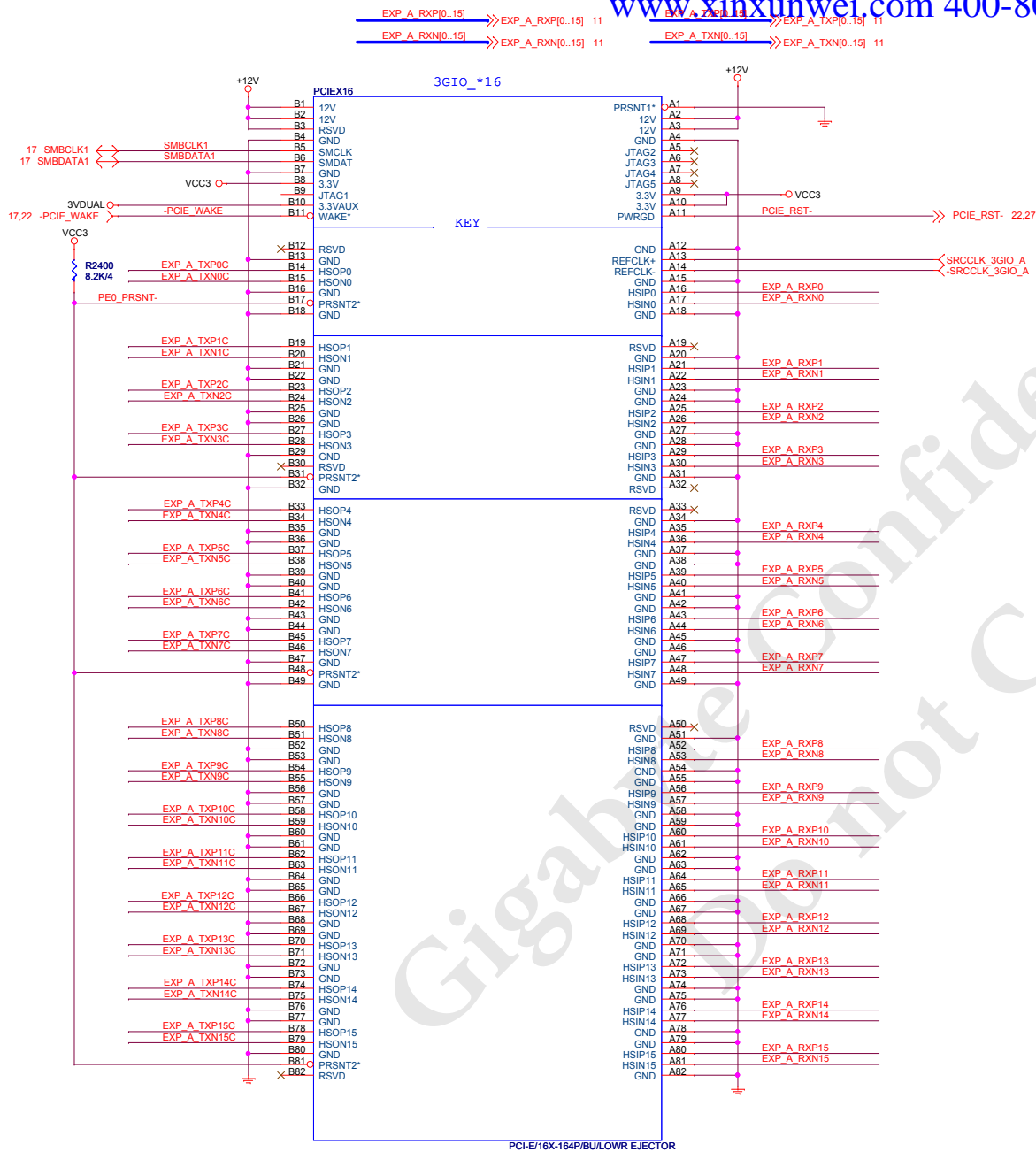


NOTE:
R650 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

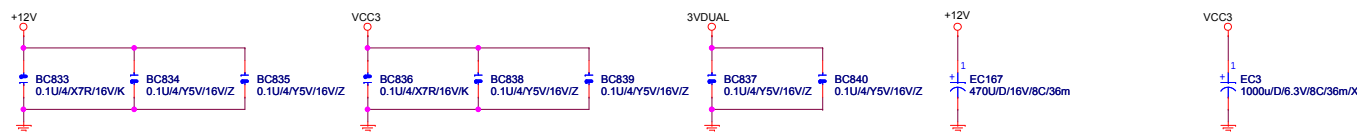
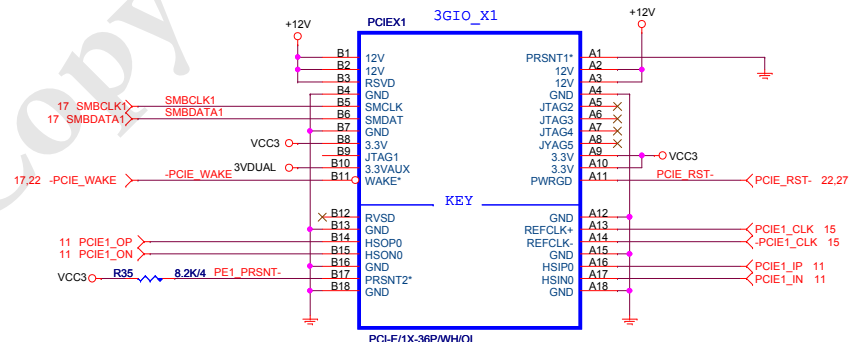


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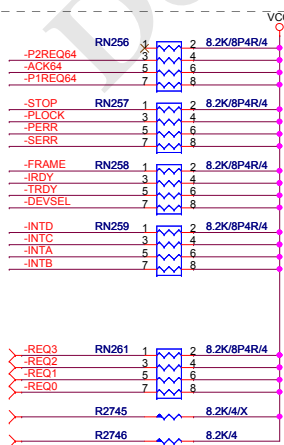
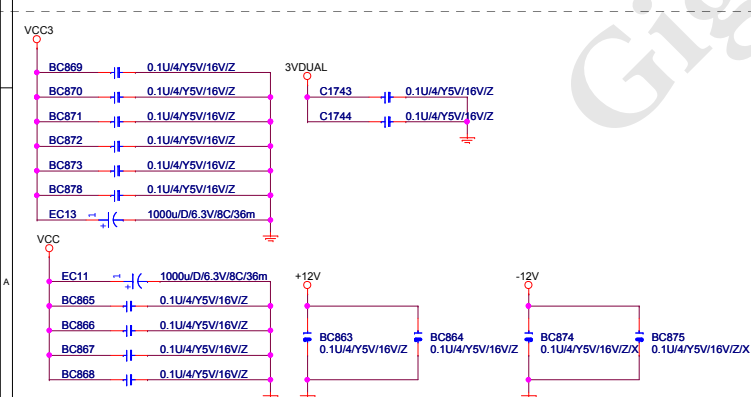
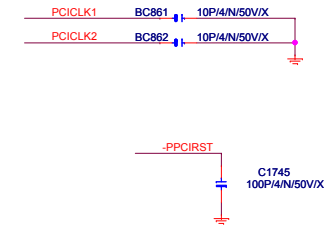
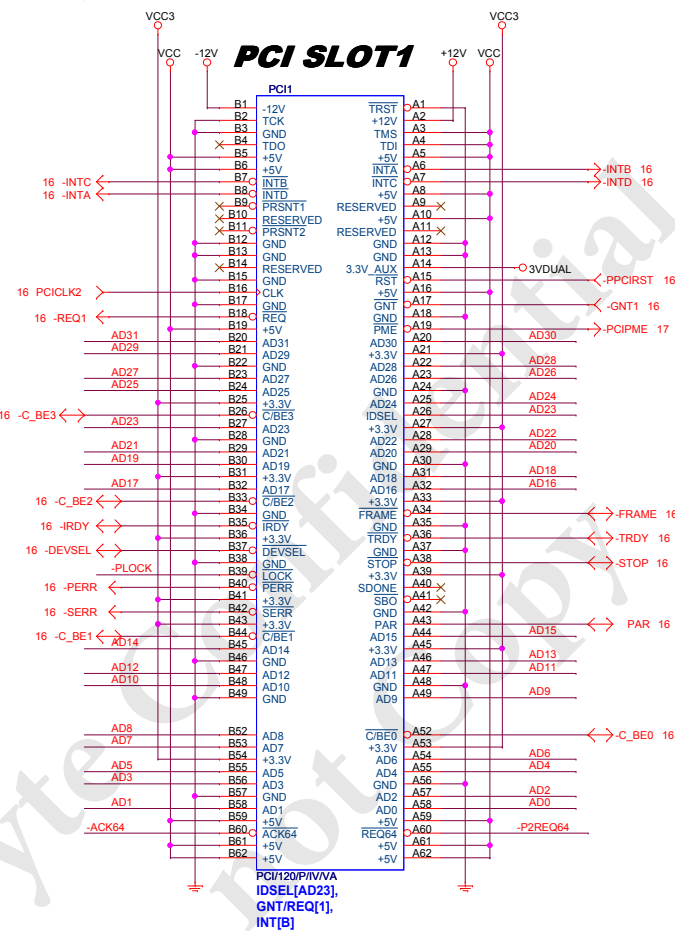
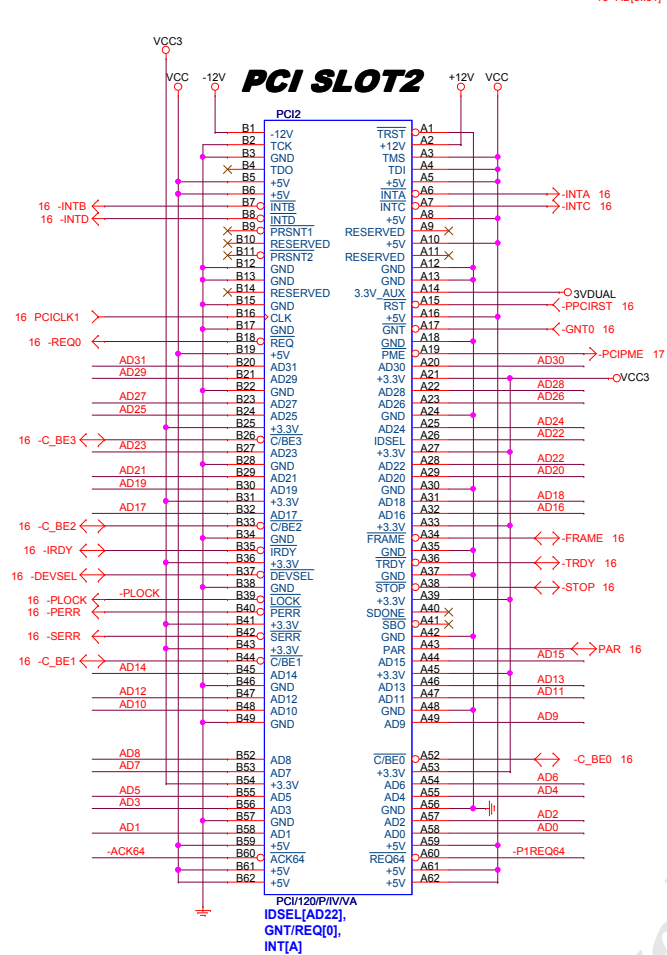
Title		
ATI SB710 SATA/IDE/HWM/SPI		
Size		
Custom	Document Number	Rev
GA-MA74GMT-S2		1.0
Date		
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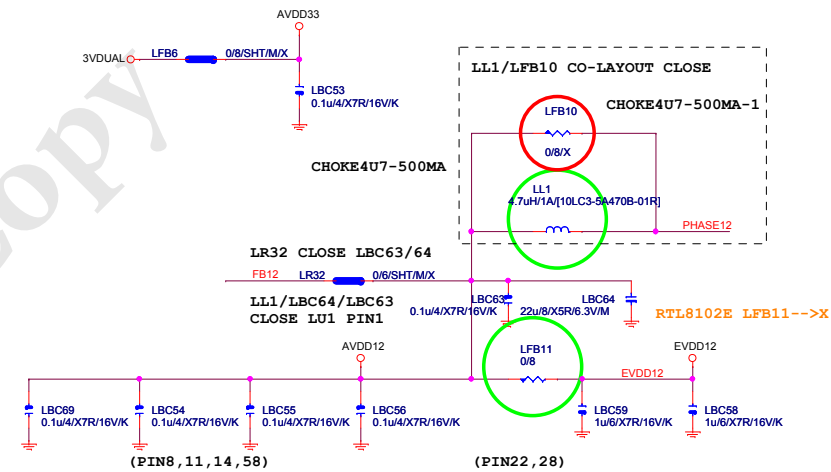
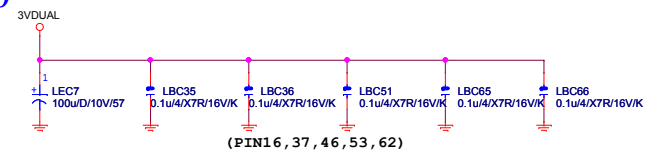


EXP A TXP0	C1644	0.1U4/XTR1/16VK	EXP A TXP0C
EXP A TXN0	C1645	0.1U4/XTR1/16VK	EXP A TXN0C
EXP A XP1	C1646	0.1U4/XTR1/16VK	EXP A XP1C
EXP A XN1	C1647	0.1U4/XTR1/16VK	EXP A XN1C
EXP A XP2	C1648	0.1U4/XTR1/16VK	EXP A XP2C
EXP A XN2	C1649	0.1U4/XTR1/16VK	EXP A XN2C
EXP A XP3	C1650	0.1U4/XTR1/16VK	EXP A XP3C
EXP A XN3	C1651	0.1U4/XTR1/16VK	EXP A XN3C
EXP A XP4	C1652	0.1U4/XTR1/16VK	EXP A XP4C
EXP A TXN4	C1653	0.1U4/XTR1/16VK	EXP A TXN4C
EXP A XP5	C1654	0.1U4/XTR1/16VK	EXP A XP5C
EXP A XN5	C1655	0.1U4/XTR1/16VK	EXP A XN5C
EXP A XP6	C1656	0.1U4/XTR1/16VK	EXP A XP6C
EXP A XN6	C1657	0.1U4/XTR1/16VK	EXP A XN6C
EXP A XP7	C1658	0.1U4/XTR1/16VK	EXP A XP7C
EXP A XN7	C1659	0.1U4/XTR1/16VK	EXP A XN7C
EXP A XP8	C1660	0.1U4/XTR1/16VK	EXP A XP8C
EXP A XN8	C1661	0.1U4/XTR1/16VK	EXP A XN8C
EXP A XP9	C1662	0.1U4/XTR1/16VK	EXP A XP9C
EXP A XN9	C1663	0.1U4/XTR1/16VK	EXP A XN9C
EXP A XP10	C1664	0.1U4/XTR1/16VK	EXP A XP10C
EXP A XN10	C1665	0.1U4/XTR1/16VK	EXP A XN10C
EXP A XP11	C1666	0.1U4/XTR1/16VK	EXP A XP11C
EXP A XN11	C1667	0.1U4/XTR1/16VK	EXP A XN11C
EXP A XP12	C1668	0.1U4/XTR1/16VK	EXP A XP12C
EXP A XN12	C1669	0.1U4/XTR1/16VK	EXP A XN12C
EXP A XP13	C1670	0.1U4/XTR1/16VK	EXP A XP13C
EXP A XN13	C1671	0.1U4/XTR1/16VK	EXP A XN13C
EXP A XP14	C1672	0.1U4/XTR1/16VK	EXP A XP14C
EXP A XN14	C1673	0.1U4/XTR1/16VK	EXP A XN14C
EXP A XP15	C1674	0.1U4/XTR1/16VK	EXP A XP15C
EXP A XN15	C1675	0.1U4/XTR1/16VK	EXP A XN15C



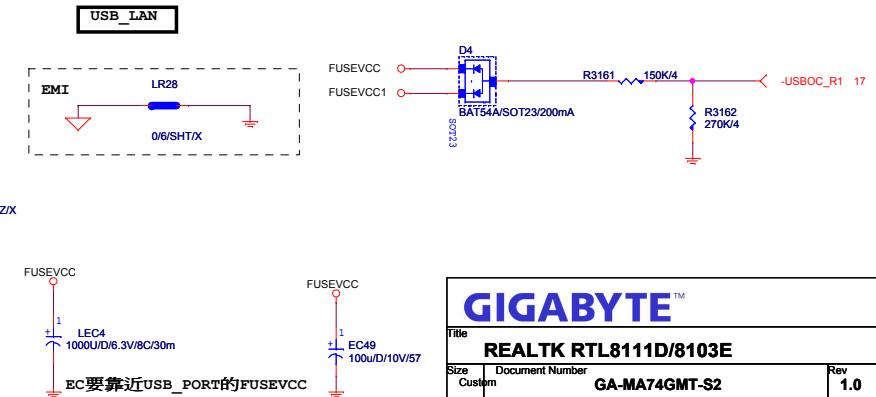
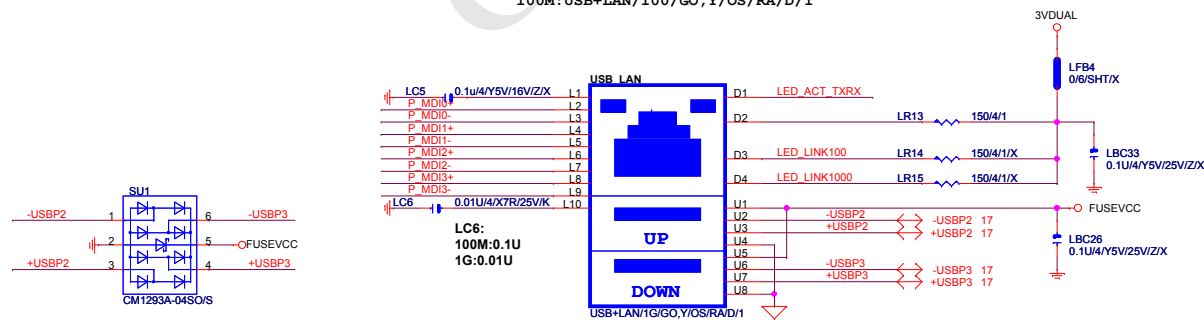
PCI SLOT 1,2

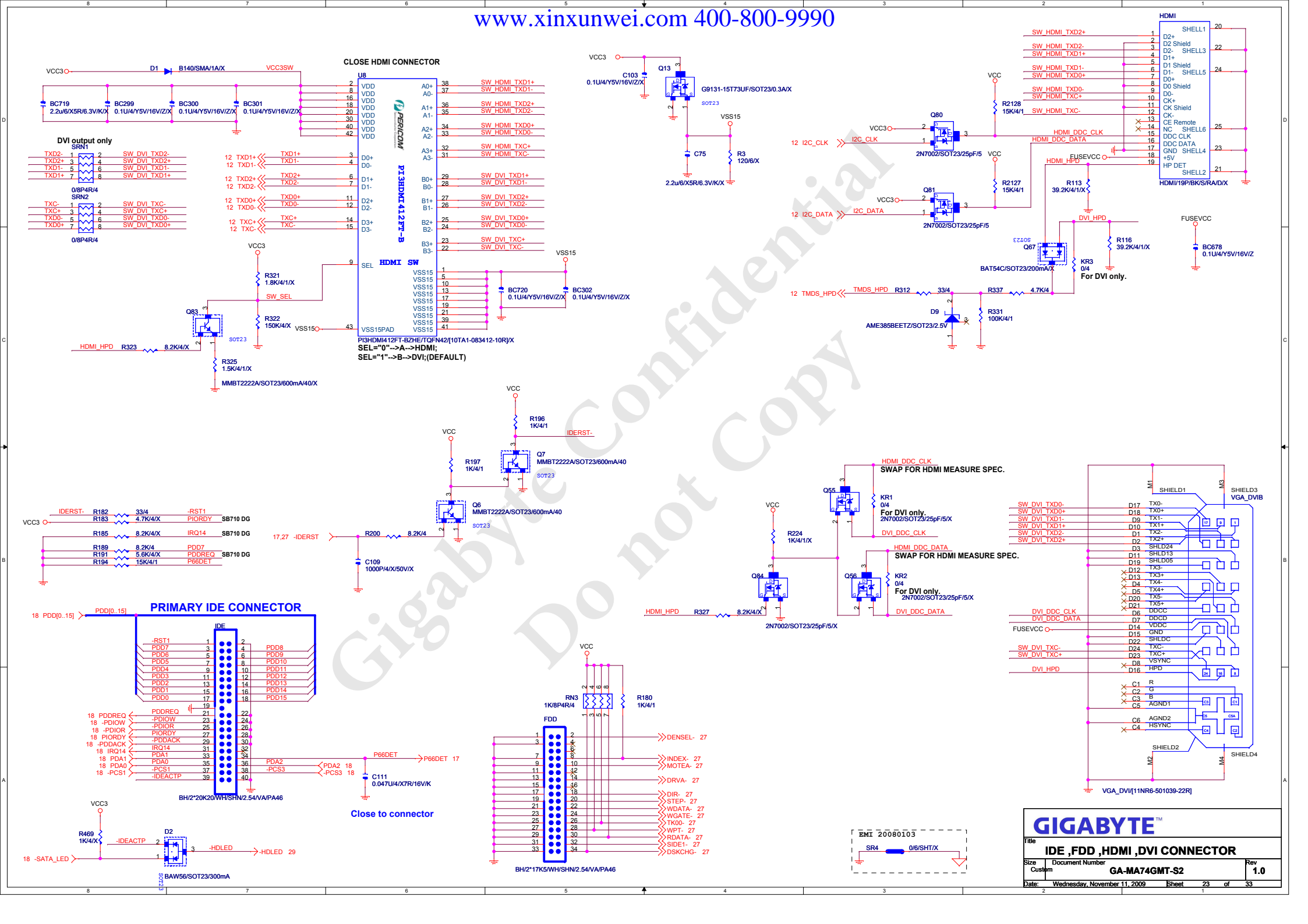


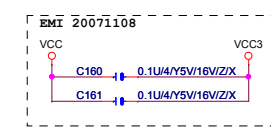
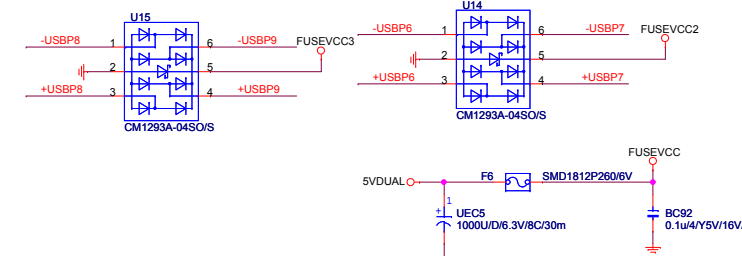
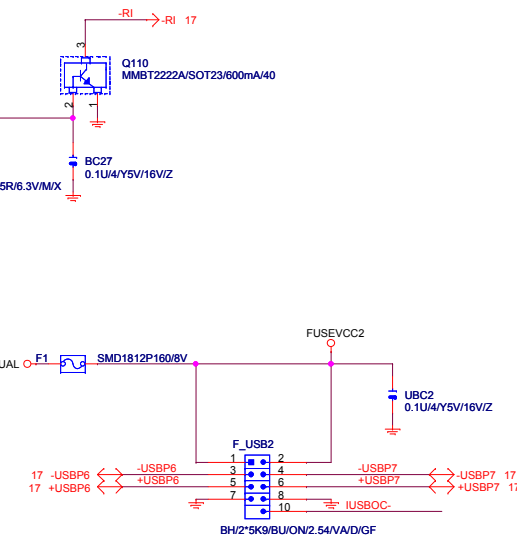
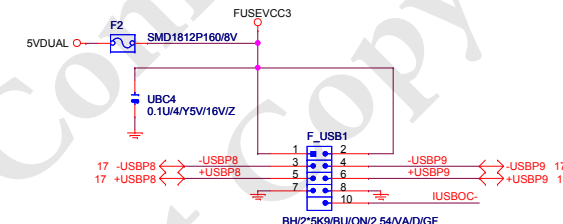
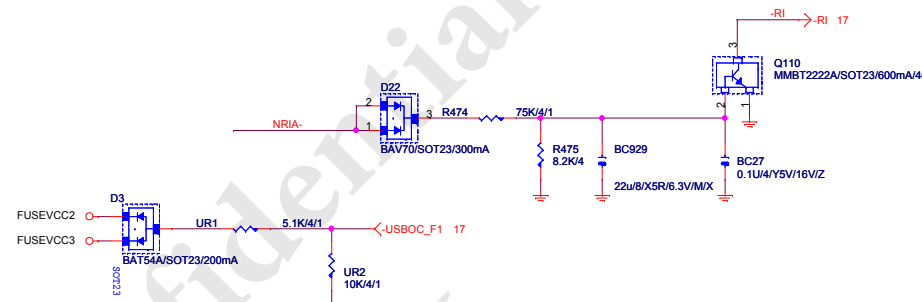
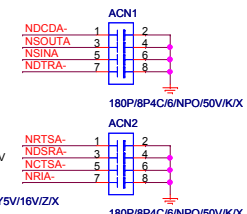
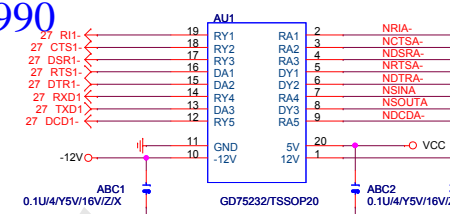
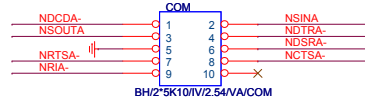
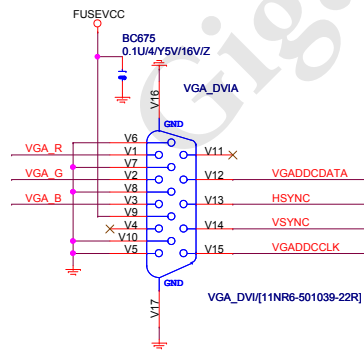
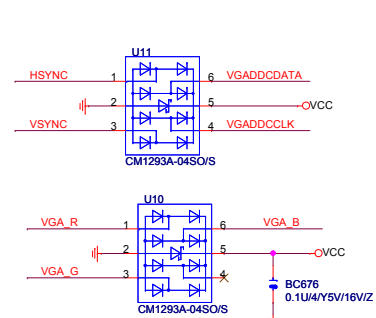
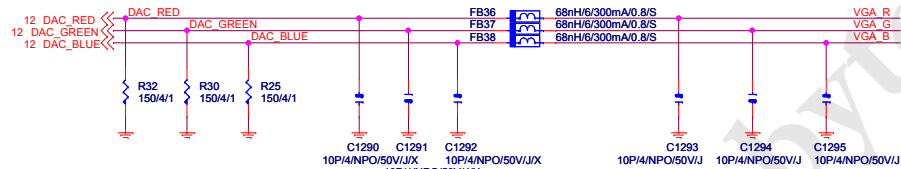
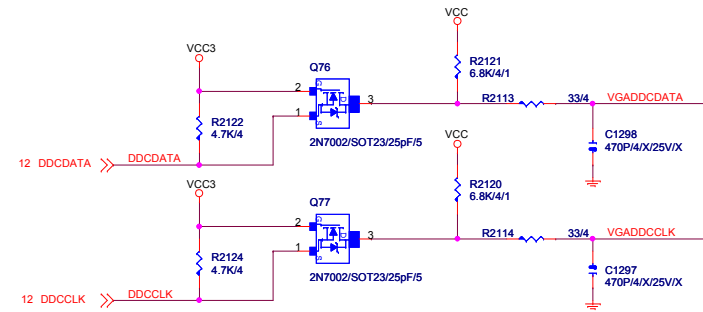
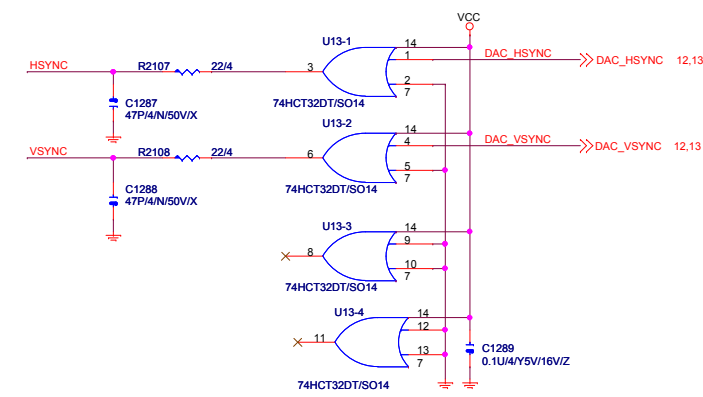


USB_LAN CONNECTOR

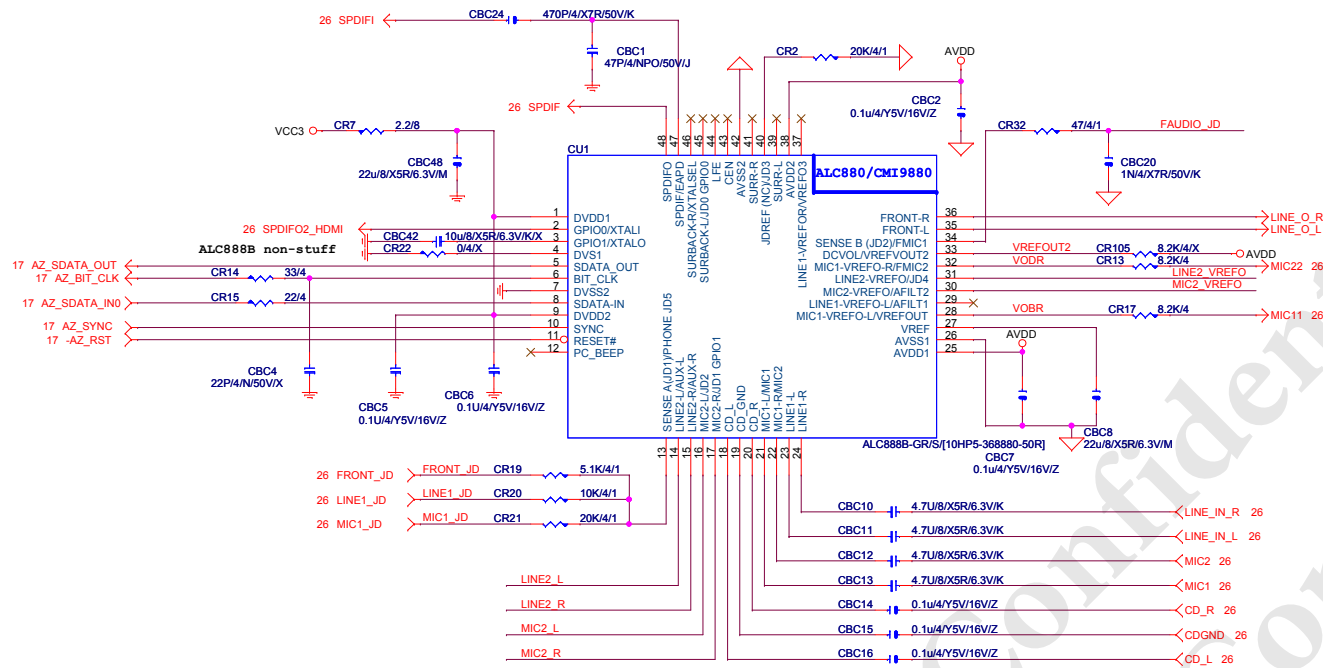
```
1G :USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1
```



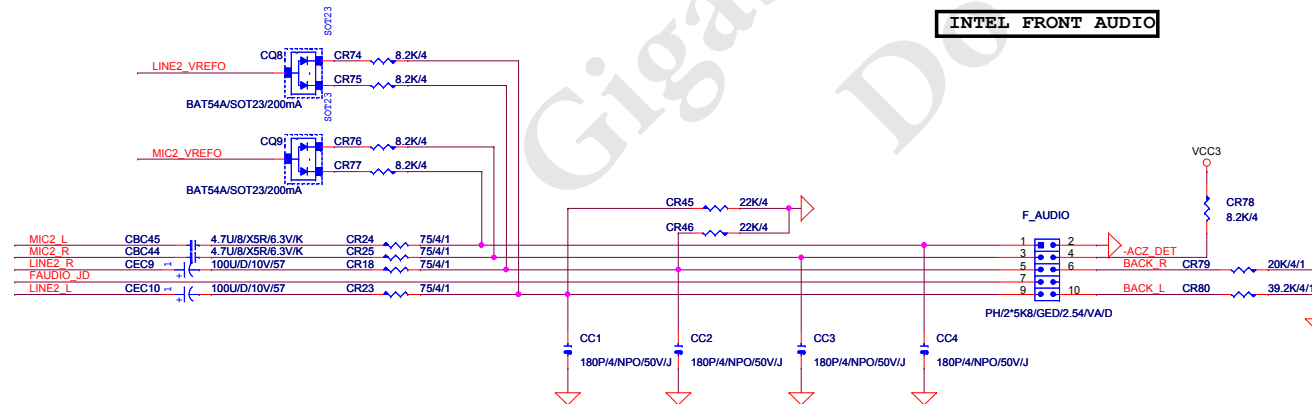




	ALC892	ALC888B
CR22	X	X
CBC42	10uF/X5R	X
CR12	O	X
CR16	X	O

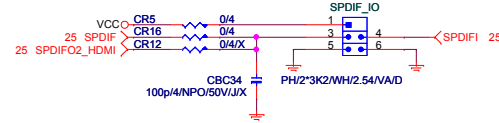
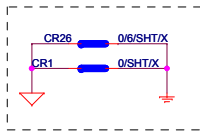


INTEL FRONT AUDIO

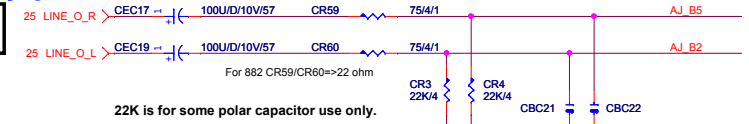


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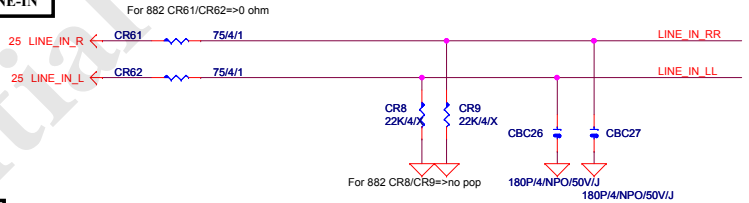


LINE OUT
FRONT OUT

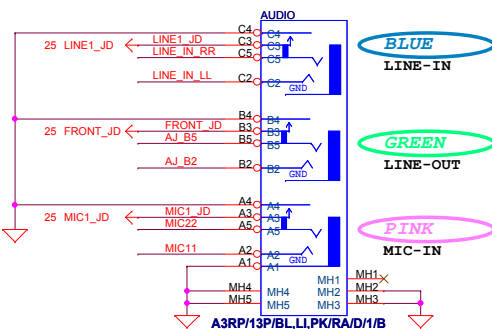
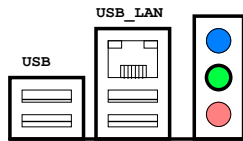
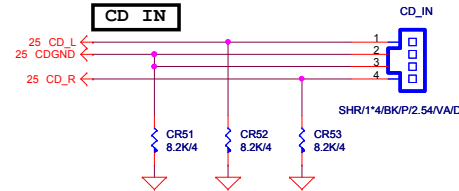
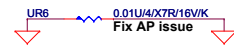
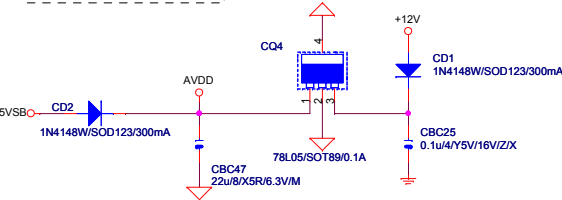
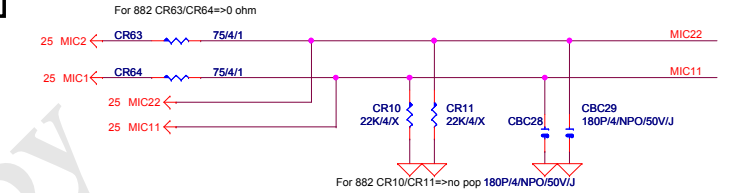


22K is for some polar capacitor use only.

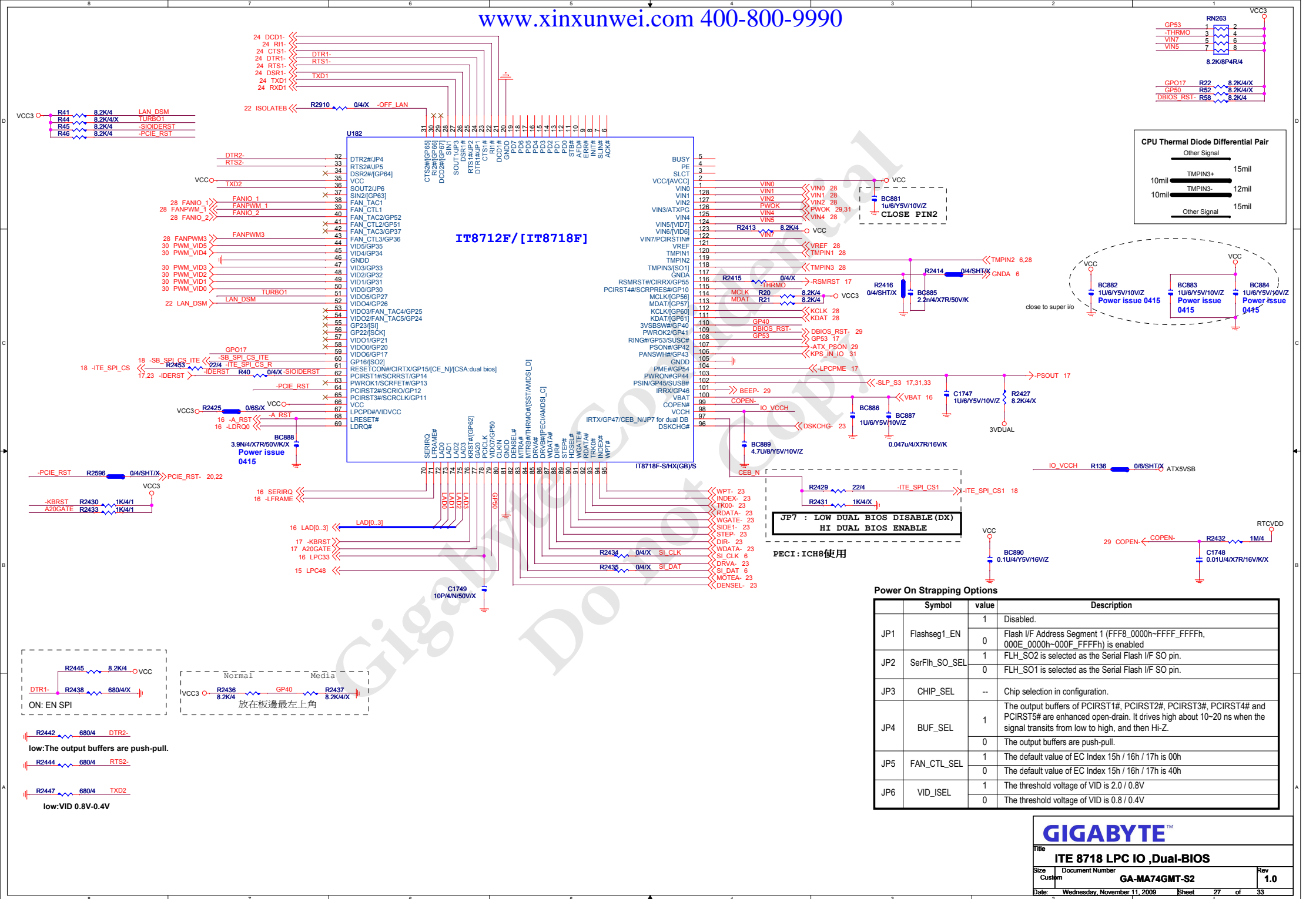
LINE-IN

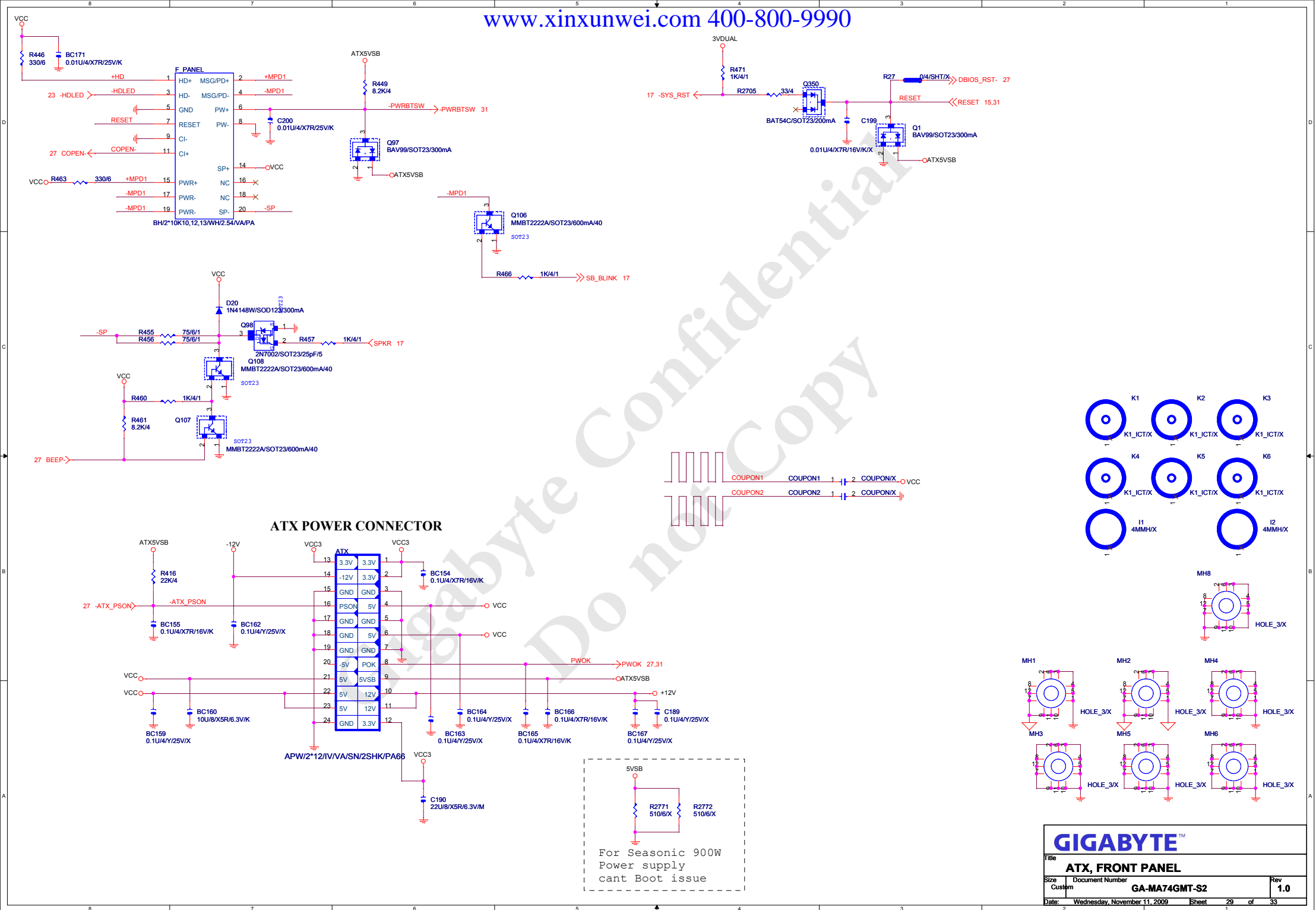


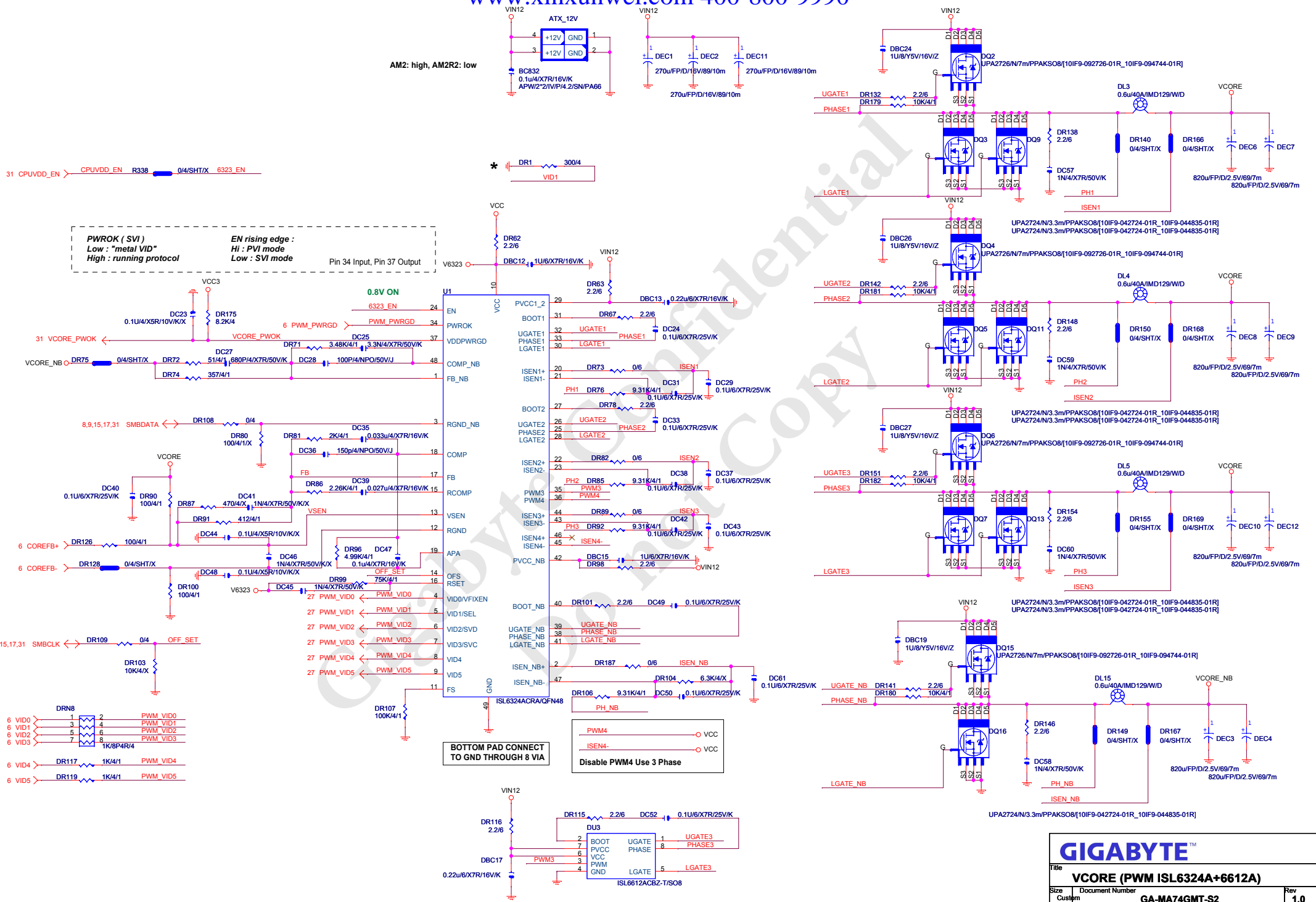
MIC



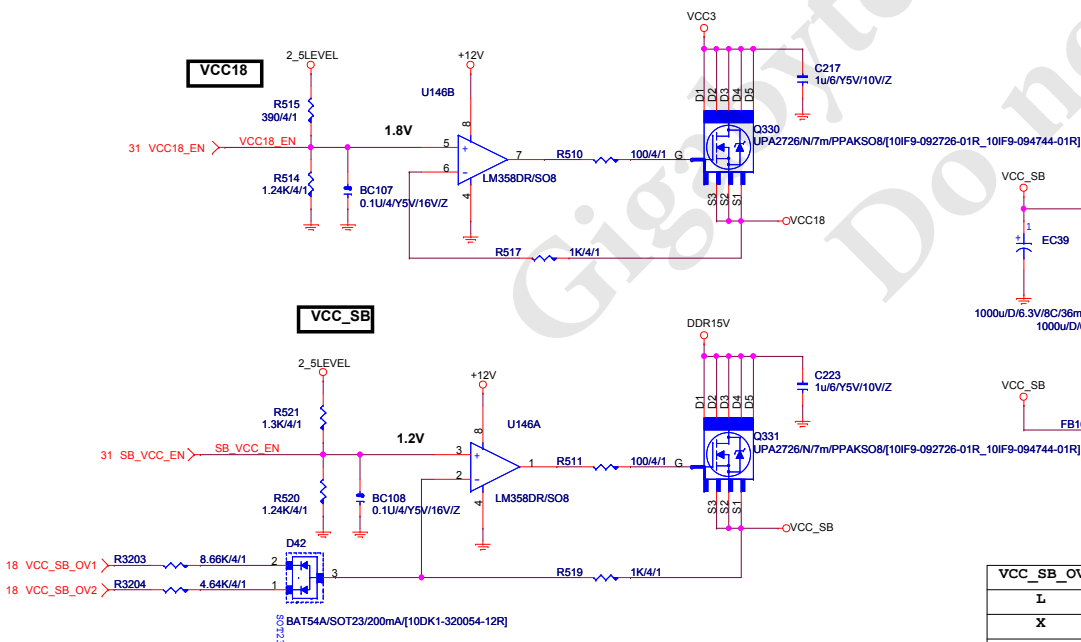
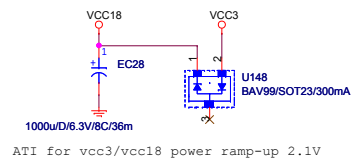
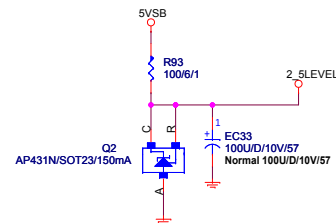
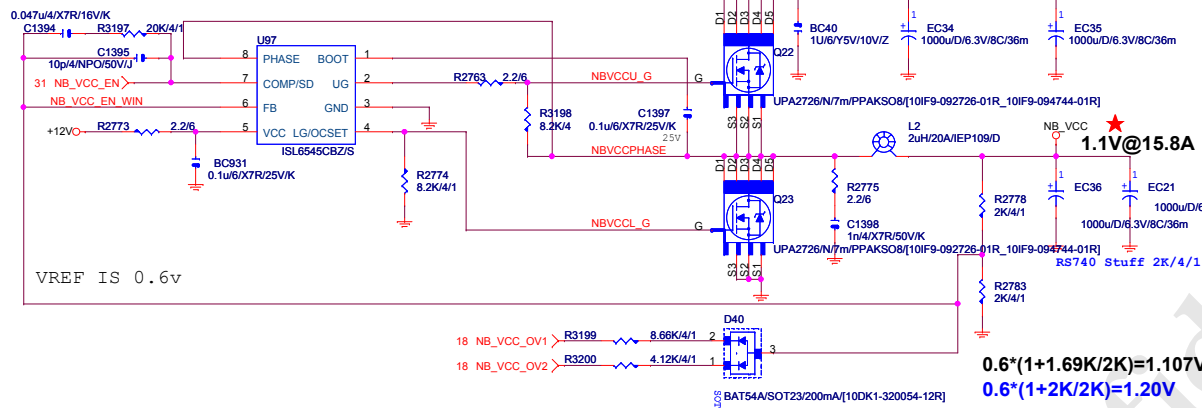
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Title			
AUDIO JACK			
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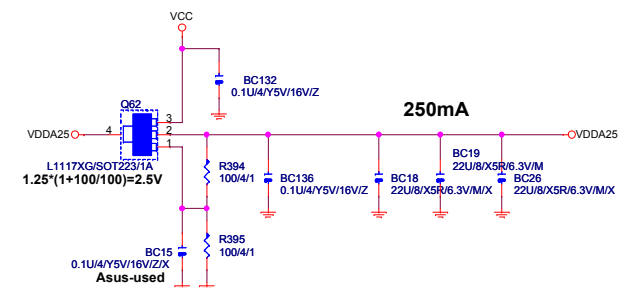
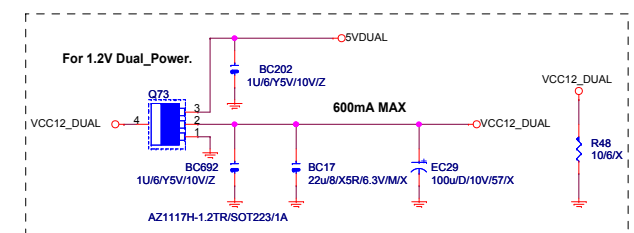




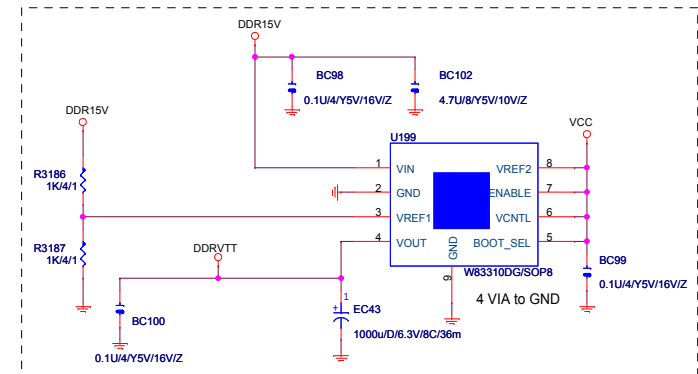
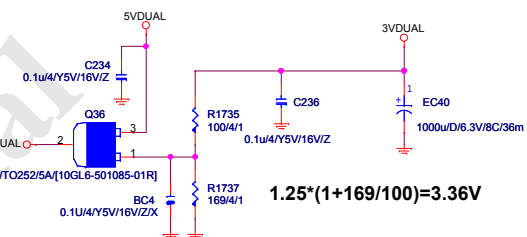




VCC_SB_OV1	VCC_SB_OV2	VCC_SB
L	X	1.30V
X	L	1.40V
L	L	1.50V


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NB/SB POWER,VCC12HT,VDDA25,VCC12Dual
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18 DDR18V_OV1 R3207 13K4/1 2 3 BAT54A/SOT23/200mA/[10DK1-320054-12R]

18 DDR18V_OV2 R3208 7.15K4/1 1 3 BAT54A/SOT23/200mA/[10DK1-320054-12R]

18 DDR18V_OV3 R3209 3.48K4/1 2 3 BAT54A/SOT23/200mA/[10DK1-320054-12R]

18 DDR18V_OV4 R3210 1.6K4/1 1 3 BAT54A/SOT23/200mA/[10DK1-320054-12R]

D45

DDR18V_OV1

L

DDR18V_OV1	DDR18V_OV2	DDR18V_OV3	DDR18V_OV4	DDR15V
X	X	X	L	2.00V
L	X	X	L	2.05V
X	L	X	L	2.10V
L	L	X	L	2.15V
X	X	L	L	2.20V
L	X	L	L	2.25V
X	L	L	L	2.30V
L	L	L	L	2.35V